RELIABILITY REPORT

FOR

ICM7555IxA

PLASTIC ENCAPSULATED DEVICES

December 8, 2004

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Quality Assurance
Reliability Lab Manager

Conclusion

The ICM7555 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The ICL7555 is a single general purpose RC Timer capable of generating accurate time delays or frequencies. The primary feature is an extremely low supply current, making this ideal for battery-powered systems. Additional features include low THRESHOLD, /RESET and /TRIGGER currents, a wide operating supply voltage range, and improved performance at high frequencies.

This CMOS lo-power devices offers significant performance over the standard 555 bipolar timer. Low-power consumption, combined with the virtually non-existent current spike during output transitions, make these timers the optimal solution in many applications.

B. Absolute Maximum Ratings

Item	Rating
Supply Voltage	+18V
Output Current	100mA
Operating Temperature Range	-20°C to +85°C
Storage Temperature Range	-65°C to +160°C
Lead Temperature (soldering, 10sec)	+300°C

II. Manufacturing Information

A. Description/Function:	General Purpose Timer
B. Process:	SMG (M6-Standard 6 micron metal gate CMOS)
C. Number of Device Transistors:	38
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Philippines, Malaysia, or Thailand
F. Date of Initial Production:	December, 1988

III. Packaging Information

	8-Lead SO	**8-Lead PDIP**
A. Package Type:		
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate or 100% Matte Tin	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-1001-0058	# 05-1001-0057
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C:	Level 1	Level 1

IV. Die Information

A. Dimensions:	44 x 54 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	6 microns (as drawn)
F. Minimum Metal Spacing:	6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Rel Operations)
Bryan Preeshl (Managing Director of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{4.04}{192 \times 4389 \times 1199 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 0.92 \times 10^{-9}$ λ = 0.92 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-1828) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1N**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The TC01 die type has been found to have all pins able to withstand a transient pulse of ±1000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±50mA.

Table 1
Reliability Evaluation Test Results

ICM7555IxA

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		1199	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	PDIP NSO	77 77	0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

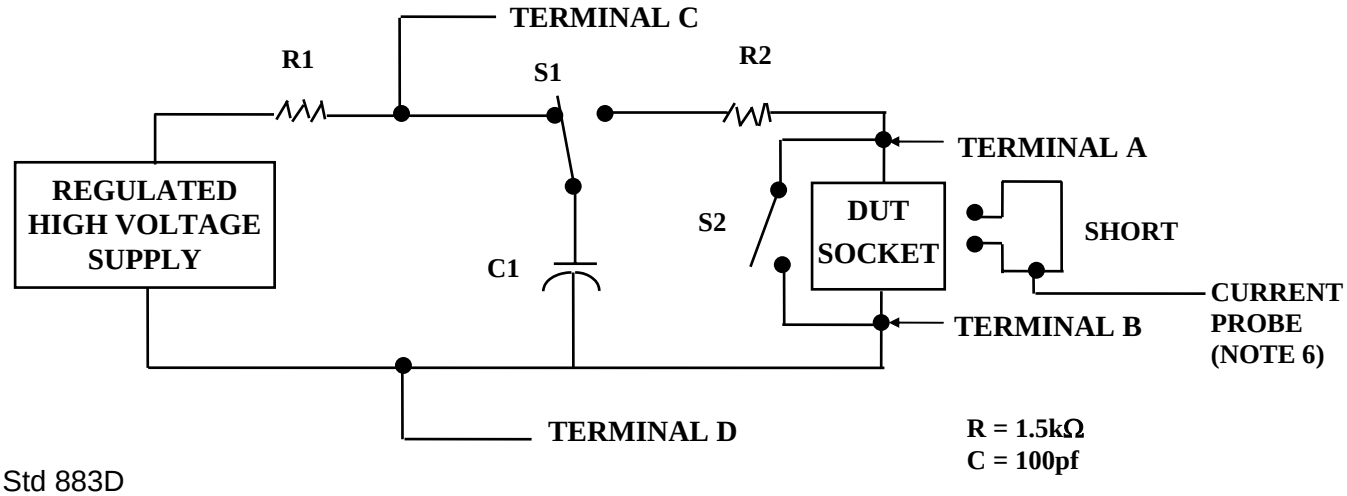
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

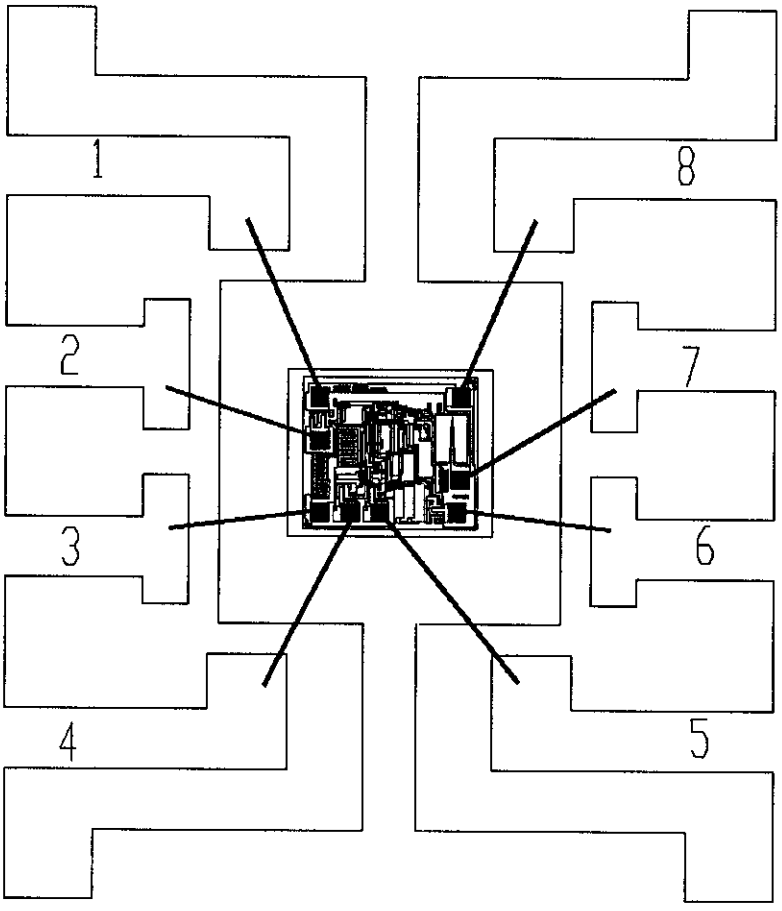
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

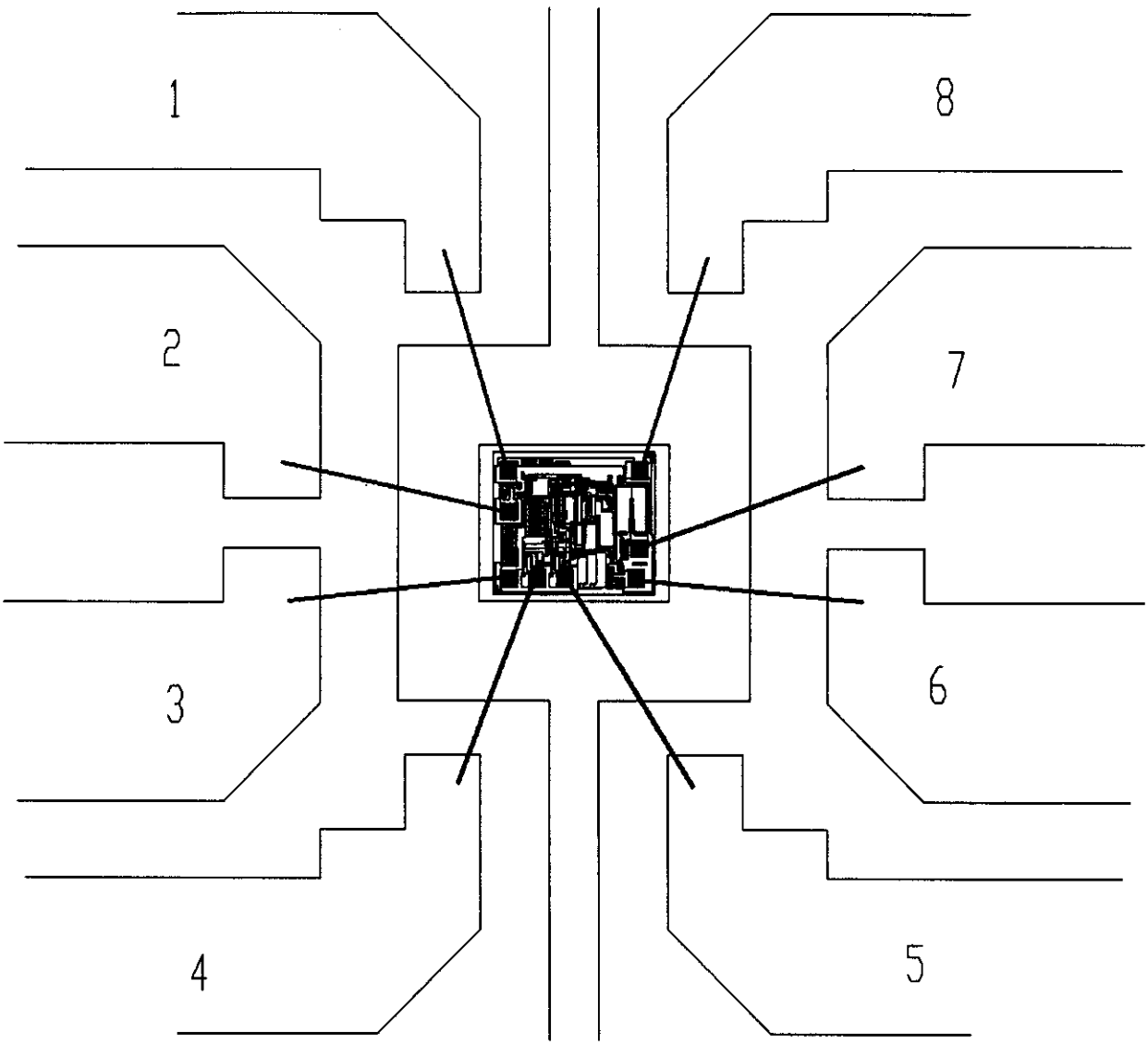
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





PKG.CODE: S8-2		APPROVALS	DATE	MAXIM	
CAV./PAD SIZE: 90 X 90	PKG. DESIGN			BUILDSHEET NUMBER: 05-1001-0058	REV.: A

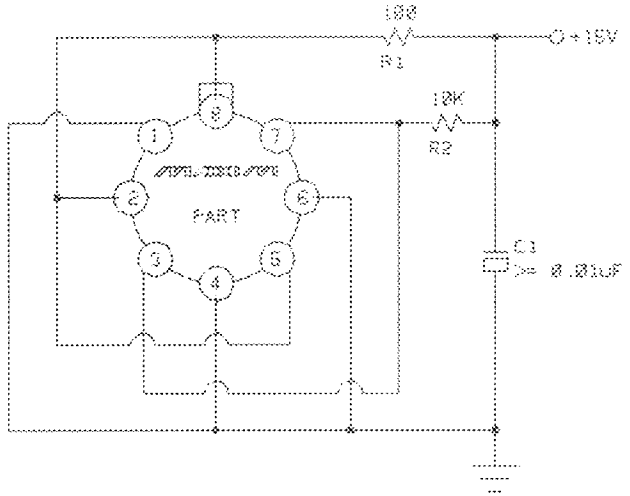


PKG.CODE: P8-1		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 100 X 100	PKG. DESIGN			BUILDSHEET NUMBER: 05-1001-0057 / REV.: A

USED FOR: ICM7555

ONCE PER BOARD

ONCE PER SOCKET



+5V I=
-5V I=
+10V I=
-10V I=
+15V I= 2mA
-15V I=
+20V I=
-20V I=
CLK1 FREQ= AMP=
CLK2 FREQ= AMP=
CLK3 FREQ= AMP=
CLK4 FREQ= AMP=
GND

- STEADY STATE LIFE TEST IS PER MIL-STD-883 METHOD 1005.
- BURN-IN IS PER MIL-STD-883 METHOD 1015. COND. B

NOTES:

1. TEMPERATURE: 125C OR EQUIVALENT
2. TIME: 160 HOURS MIN. OR EQUIVALENT
3. ALL COMPONENTS AND MATERIAL MUST STAND 150C CONTINUOUS
4. APPROVED FOR [X] COMMERCIAL
   [X] MR/883

SPEC. NO. 06-1020 REV. B

DATE: 5/7/92

MAXIM BURN-IN SCHEMATIC

APPROVAL DATE: 7-29-92