

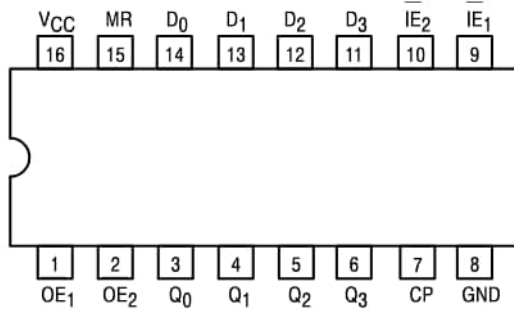


# 4-BIT D-TYPE REGISTER WITH 3-STATE OUTPUTS

The SN54/74LS173A is a high-speed 4-Bit Register featuring 3-state outputs for use in bus-organized systems. The clock is fully edge-triggered allowing either a load from the D inputs or a hold (retain register contents) depending on the state of the Input Enable Lines (IE<sub>1</sub>, IE<sub>2</sub>). A HIGH on either Output Enable line (OE<sub>1</sub>, OE<sub>2</sub>) brings the output to a high impedance state without affecting the actual register contents. A HIGH on the Master Reset (MR) input resets the Register regardless of the state of the Clock (CP), the Output Enable (OE<sub>1</sub>, OE<sub>2</sub>) or the Input Enable (IE<sub>1</sub>, IE<sub>2</sub>) lines.

- Fully Edge-Triggered
- 3-State Outputs
- Gated Input and Output Enables
- Input Clamp Diodes Limit High-Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

**PIN NAMES**

D <sub>0</sub> -D <sub>3</sub>	Data Inputs
IE <sub>1</sub> -IE <sub>2</sub>	Input Enable (Active LOW)
OE <sub>1</sub> -OE <sub>2</sub>	Output Enable (Active LOW) Inputs
CP	Clock Pulse (Active HIGH Going Edge) Input
MR	Master Reset Input (Active HIGH)
Q <sub>0</sub> -Q <sub>3</sub>	Outputs (Note b)

**LOADING (Note a)**

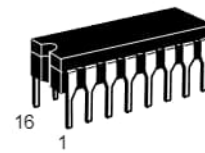
	HIGH	LOW
D <sub>0</sub> -D <sub>3</sub>	0.5 U.L.	0.25 U.L.
IE <sub>1</sub> -IE <sub>2</sub>	0.5 U.L.	0.25 U.L.
OE <sub>1</sub> -OE <sub>2</sub>	0.5 U.L.	0.25 U.L.
CP	0.5 U.L.	0.25 U.L.
MR	0.5 U.L.	0.25 U.L.
Q <sub>0</sub> -Q <sub>3</sub>	65 (25) U.L.	15 (7.5) U.L.

**NOTES:**

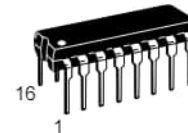
- a. 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.  
 b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

## SN54/74LS173A

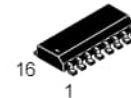
### 4-BIT D-TYPE REGISTER WITH 3-STATE OUTPUTS LOW POWER SCHOTTKY



**J SUFFIX**  
CERAMIC  
CASE 620-09



**N SUFFIX**  
PLASTIC  
CASE 648-08

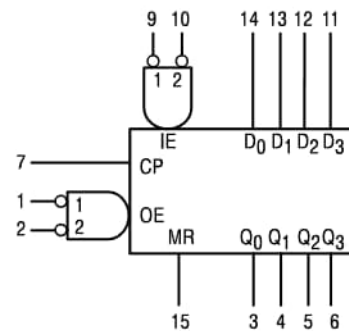


**D SUFFIX**  
SOIC  
CASE 751B-03

**ORDERING INFORMATION**

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

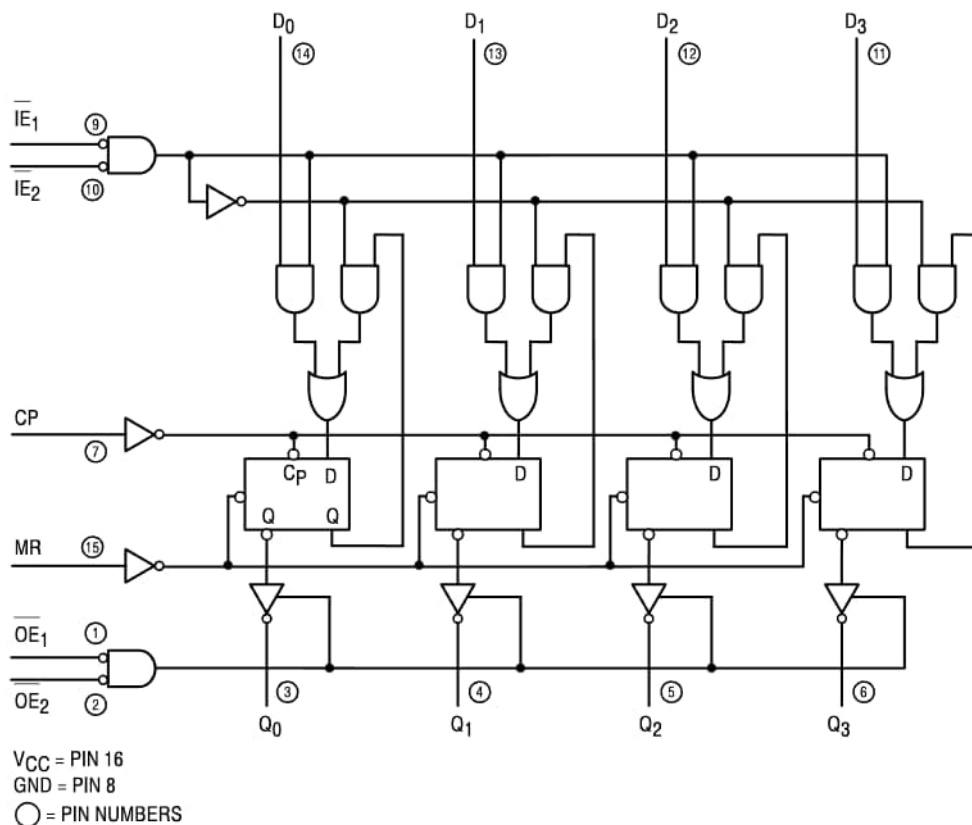
**LOGIC SYMBOL**



VCC = PIN 16  
GND = PIN 8

# SN54/74LS173A

## LOGIC DIAGRAM



TRUTH TABLE

MR	CP	IE <sub>1</sub>	IE <sub>2</sub>	D <sub>n</sub>	Q <sub>n</sub>
H	x	x	x	x	L
L	L	x	x	x	Q <sub>n</sub>
L	↯	H	x	x	Q <sub>n</sub>
L	↯	x	H	x	Q <sub>n</sub>
L	↯	L	L	L	L
L	↯	L	L	H	H

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial

When either OE<sub>1</sub>, or OE<sub>2</sub> are HIGH, the output is in the off state (High Impedance); however this does not affect the contents or sequential operation of the register.

## GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T <sub>A</sub>	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I <sub>OH</sub>	Output Current — High	54			-1.0	mA
		74			-2.6	
I <sub>OL</sub>	Output Current — Low	54			12	mA
		74			24	

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## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V <sub>IL</sub>	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA	
V <sub>OH</sub>	Output HIGH Voltage	54	2.4	3.4	V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table	
		74	2.4	3.1	V		
V <sub>OL</sub>	Output LOW Voltage	54, 74		0.25	0.4	V	I <sub>OL</sub> = 12 mA V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table
		74		0.35	0.5	V	
I <sub>OZH</sub>	Output Off Current HIGH			20	αA	V <sub>CC</sub> = MAX, V <sub>O</sub> = 2.7 V	
I <sub>OZL</sub>	Output Off Current LOW			-20	αA	V <sub>CC</sub> = MAX, V <sub>O</sub> = 0.4 V	
I <sub>IH</sub>	Input HIGH Current			20	αA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V	
				0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V	
I <sub>IL</sub>	Input LOW Current			-0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V	
I <sub>OS</sub>	Short Circuit Current (Note 1)	-30		-130	mA	V <sub>CC</sub> = MAX	
I <sub>CC</sub>	Power Supply Current			30	mA	V <sub>CC</sub> = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f <sub>MAX</sub>	Maximum Input Clock Frequency	30	50		MHz	V <sub>CC</sub> = 5.0 V C <sub>L</sub> = 45 pF, R <sub>L</sub> = 667 Ω
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, Clock to Output		17 22	25 30	ns	
t <sub>PHL</sub>	Propagation Delay, MR to Output		26	35	ns	
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time		15 18	23 27	ns	
t <sub>PLZ</sub> t <sub>PHZ</sub>	Output Disable Time		11 11	17 17	ns	C <sub>L</sub> = 5.0 pF, R <sub>L</sub> = 667 Ω

## AC SETUP REQUIREMENTS (T<sub>A</sub> = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t <sub>W</sub>	Clock or MR Pulse Width	20			ns	V <sub>CC</sub> = 5.0 V
t <sub>S</sub>	Data Enable Setup Time	35			ns	
t <sub>S</sub>	Data Setup Time	17			ns	
t <sub>H</sub>	Hold Time, Any Input	0			ns	
t <sub>rec</sub>	Recovery Time	10			ns	

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## AC WAVEFORMS

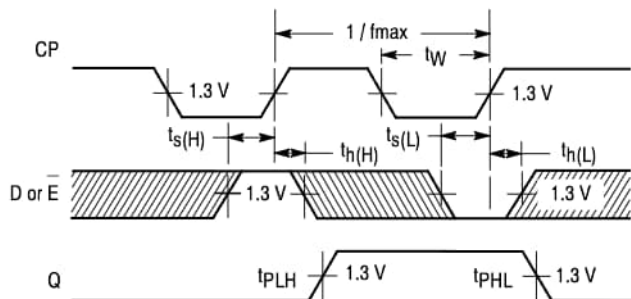


Figure 1

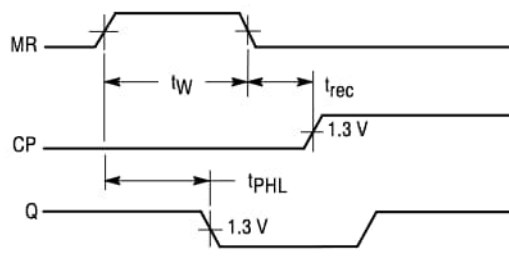


Figure 2

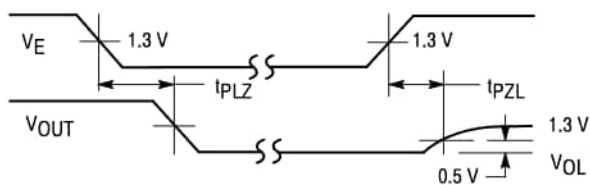


Figure 3

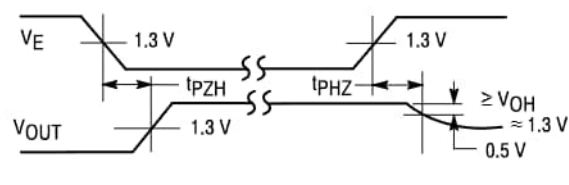
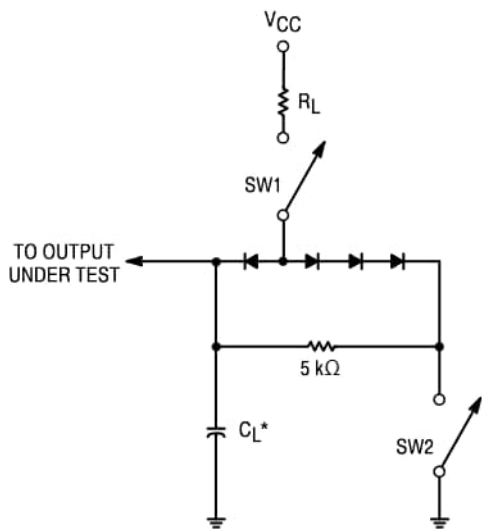


Figure 4

## AC LOAD CIRCUIT



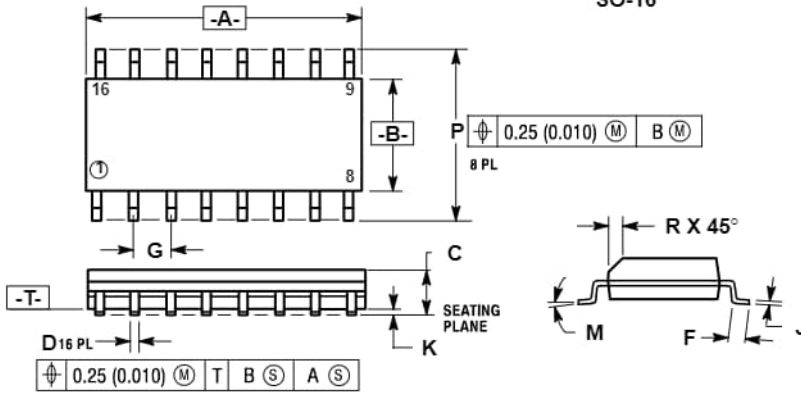
\*Includes Jig and Probe Capacitance.

Figure 5

### SWITCH POSITIONS

SYMBOL	SW1	SW2
$t_{PZH}$	Open	Closed
$t_{PZL}$	Closed	Open
$t_{PLZ}$	Closed	Closed
$t_{PHZ}$	Closed	Closed

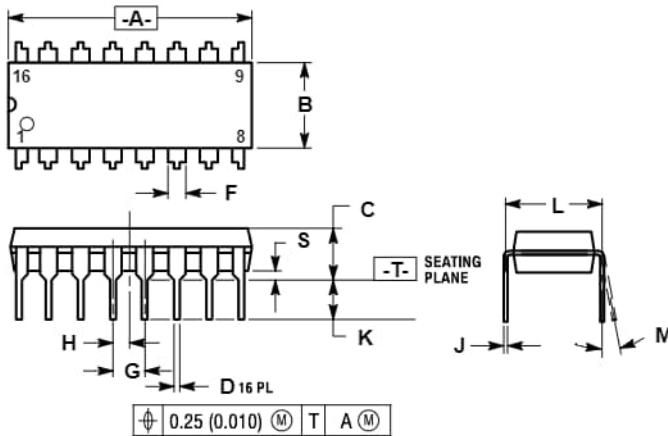
Case 751B-03 D Suffix  
16-Pin Plastic  
SO-16



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. 751B-01 IS OBSOLETE, NEW STANDARD 751B-03.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

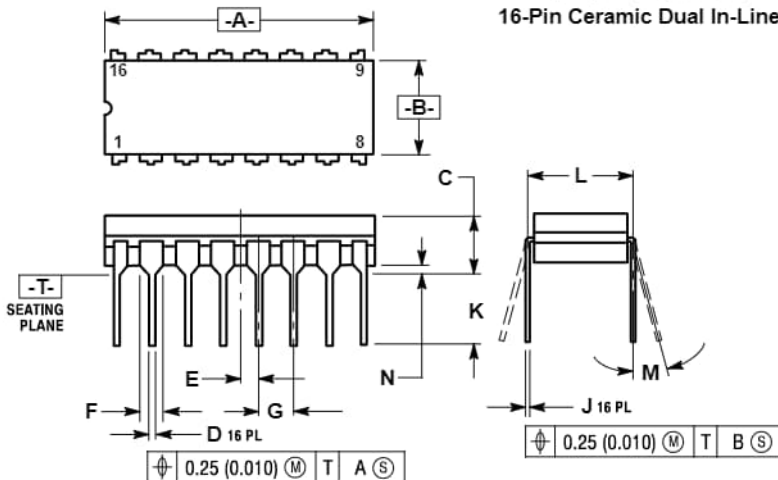
Case 648-08 N Suffix  
16-Pin Plastic



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
  4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
  5. ROUNDED CORNERS OPTIONAL.
  6. 648-01 THRU -07 OBSOLETE, NEW STANDARD 648-08.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	19.55	0.740	0.770
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.39	0.53	0.015	0.021
F	1.02	1.77	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.27 BSC		0.050 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.30	0.110	0.130
L	7.50	7.74	0.295	0.305
M	0°	10°	0°	10°
S	0.51	1.01	0.020	0.040

Case 620-09 J Suffix  
16-Pin Ceramic Dual In-Line



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
  4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.
  5. 620-01 THRU -08 OBSOLETE, NEW STANDARD 620-09.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.55	0.750	0.770
B	6.10	7.36	0.240	0.290
C	—		4.19	—
D	0.39	0.53	0.015	0.021
E	1.27 BSC		0.050 BSC	
F	1.40	1.77	0.055	0.070
G	2.54 BSC		0.100 BSC	
J	0.23	0.27	0.009	0.011
K	—		5.08	—
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.39	0.88	0.015	0.035

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