D8254

Programmable Interval Timer
ver 1.08

OVERVIEW

The D8254 is a programmable interval timer/counter, binary compatible with industry standard 82C54. The D8254 solves one of the most common problems in any micro-computer system, the generation of accurate time delays under software control. The D8254 can be used as a:

- Real time clock
- Even counter
- Digital one-shot
- Programmable rate generator
- Square wave generator
- Binary rate multiplier
- Complex waveform generator
- Complex motor controller

KEY FEATURES

- Three independent 16-bit counters
- Six programmable Counter modes
  - *Interrupt on terminal count*
  - *Hardware retriggerable One-Shot*
  - *Rate Generator*
  - *Square wave mode*
  - *Software triggered strobe*
  - *Hardware triggered strobe*
- Binary or BCD counting
- Status Read Back Command

- Simple interface allows easy connection to microcontrollers
- Fully synthesizable, static design with no internal tri-states

DELIVERABLES

- Source code:
  - ◊ VHDL Source Code or/and
  - ◊ VERILOG Source Code or/and
  - ◊ Encrypted, or plain text EDIF netlist
- VHDL & VERILOG test bench environment
  - ◊ Active-HDL automatic simulation macros
  - ◊ ModelSim automatic simulation macros
  - ◊ Tests with reference responses
- Technical documentation
  - ◊ Installation notes
  - ◊ HDL core specification
  - ◊ Datasheet
- Synthesis scripts
- Example application
- Technical support
  - ◊ IP Core implementation support
  - ◊ 3 months maintenance
    - Delivery the IP Core updates, minor and major versions changes
    - Delivery the documentation updates
    - Phone & email support

http://www.DigitalCoreDesign.com
http://www.dcd.pl

LICENSING

Comprehensible and clearly defined licensing methods without royalty fees make using of IP Core easy and simply.

Single Design license allows use IP Core in single FPGA bitstream and ASIC implementation.

Unlimited Designs, One Year licenses allow use IP Core in unlimited number of FPGA bitstreams and ASIC implementations.

In all cases number of IP Core instantiations within a design, and number of manufactured chips are unlimited. There is no time restriction except *One Year* license where time of use is limited to 12 months.

- Single Design license for
  - *VHDL, Verilog source code called HDL Source*
  - *Encrypted, or plain text EDIF called Netlist*
- One Year license for
  - *Encrypted Netlist only*
- Unlimited Designs license for
  - *HDL Source*
  - *Netlist*
- Upgrade from
  - *HDL Source to Netlist*
 - *Single Design to Unlimited Designs*

SYMBOL
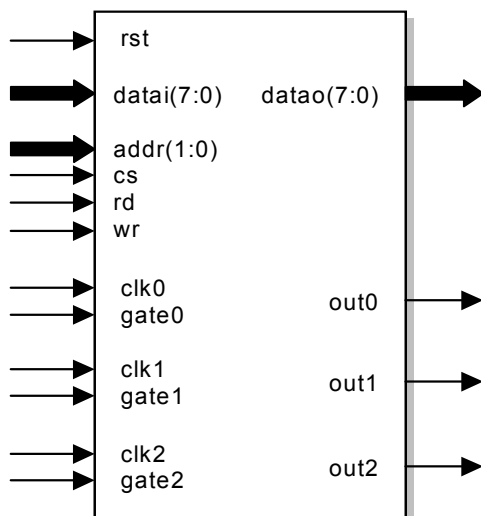
PINS DESCRIPTION

PIN	TYPE	DESCRIPTION
rst	input	Global reset
datai(7:0)	input	Processor data bus (input)
addr(1:0)	input	Processor address lines
cs	input	Chip select
rd	input	Processor read strobe
wr	input	Processor write strobe
clk0	input	Clock input for Counter 0
gate0	input	Gate input for Counter 0
clk1	input	Clock input for Counter 1
gate1	input	Gate input for Counter 1
clk2	input	Clock input for Counter 2
gate2	input	Gate input for Counter 2
datao(7:0)	output	Processor data bus (output)
out0	output	Output of Counter 0
out1	output	Output of Counter 1
out2	output	Output of Counter 2

BLOCK DIAGRAM
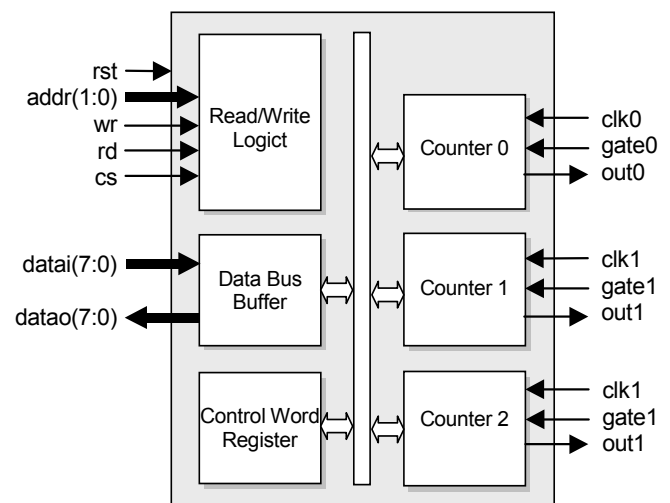
Read Write Logic - The Read/Write Logic accepts inputs from the system bus and generates control signals for the other functional blocks of the D8254. ADDR(1:0) select one of the three counters or the Control Word Register to be read from/written into. A "low" on the RD input tells the D8254 that the CPU is reading one of the counters. A "low" on the WR input tells the D8254 that the CPU is writing either a Control Word or an initial count. Both RD and WR are qualified by CS; RD and WR are ignored unless the 82C54 has

been selected by holding CS low. The WR and CLK signals should be synchronous. This is accomplished by using a CLK input signal to the D8254 counters which is a derivative of the system clock source. Another technique is to externally synchronize the WR and CLK input signals. This is done by gating WR with CLK.

**Data Bus Buffer** 8-bit buffer is used to interface the D8254 to the system bus.

Control Word - The Control Word Register is selected by the Read/Write Logic when ADDR(1:0) = 11. If the CPU then does a write operation to the D8254, the data is stored in the Control Word Register and is interpreted as a Control Word used to define the operation of the Counters.

COUNTERS BLOCK DIAGRAM

All three Counters (0, 1, 2) are functionally identical and fully independent. Each can work as a 16 bit wide Binary or BCD counter, in one of the six available modes:

- Interrupt on terminal count
- Hardware retriggerable One-Shot
- Rate Generator
- Square wave mode
- Software triggered strobe
- Hardware triggered strobe

The internal block diagram of a single counter is shown in Figure below.
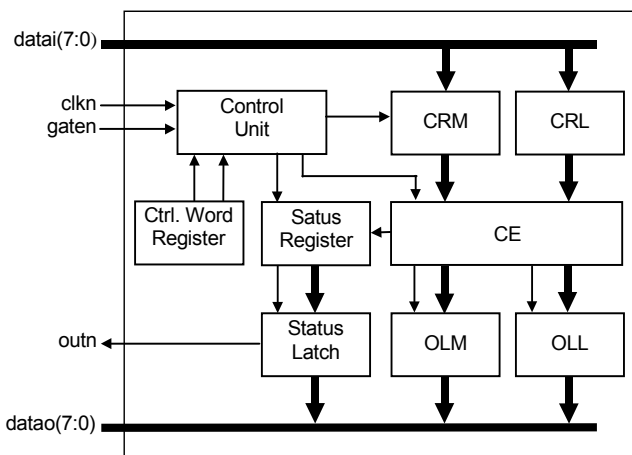
The central element of each Counter is **CE** module - Counting Element – 16 bit pre-

settable synchronous down BIN/BCD counter.

Status Register, Status Latch – Status register contains actual mode declaration and value of output signal. Latched in Status Latch, after receiving Read-Back Command with STATUS Bit = 0.

Control Unit – Controls read/write operation and decrementing of CE.

CR M, CR L – Input data registers. When new count is written to counter, the count is written in the CR and later transferred to CE.

OL L, OL M – Output data registers. Latched when the suitable Counter Latch Command is sent to the D8254.

Control Word - The Control Word Register is selected by the Read/Write Logic when ADDR(1:0) = 11. If the CPU then does a write operation to the D8254, the data is stored in the Control Word Register and is interpreted as a Control Word used to define the operation of the Counters.

PERFORMANCE

The following table gives a survey about the Core area and performance in the ALTERA® devices after Place & Route:

Device	Speed grade	Logic Cells	F_{max}
CYCLONE	-6		150 MHz
CYCLONE 2	-6		166 MHz
STRATIX	-5		181 MHz
STRATIX 2	-3		238 MHz
STRATIXGX	-5		185 MHz
MERCURY	-5		135 MHz
EXCALIBUR	-1		108 MHz
APEX II	-7		140 MHz
APEX20KC	-7		129 MHz
APEX20KE	-1		105 MHz
APEX20K	-1V		88 MHz
ACEX1K	-1		99 MHz
FLEX10KE	-1		102 MHz

Core performance in ALTERA® devices

http://www.DigitalCoreDesign.com
http://www.dcd.pl

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