Features

- **Low-voltage Operation**
  - **– 2.7 (V_{CC} = 2.7V to 5.5V)**
- **Internally Organized 131,072 x 8**
- **Two-wire Serial Interface**
- **Schmitt Triggers, Filtered Inputs for Noise Suppression**
- **Bidirectional Data Transfer Protocol**
- **400 kHz (2.7V) and 1 MHz (5V) Clock Rate**
- **Write Protect Pin for Hardware and Software Data Protection**
- **256-byte Page Write Mode (Partial Page Writes Allowed)**
- **Random and Sequential Read Modes**
- **Self-timed Write Cycle (5 ms Typical)**
- **High Reliability**
  - **– Endurance: 100,000 Write Cycles/Page**
  - **– Data Retention: 40 Years**
- **8-lead PDIP, 8-lead EIAJ SOIC, 8-lead LAP and 8-lead SAP Packages**
- **Die Sales: Wafer Form, Waffle Pack and Bumped Die**

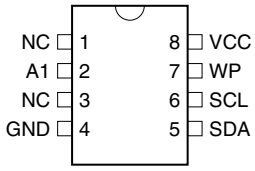
Description

The AT24C1024 provides 1,048,576 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 131,072 words of 8 bits each. The device's cascadable feature allows up to two devices to share a common two-wire bus. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The devices are available in space-saving 8-lead PDIP, 8-lead EIAJ SOIC, 8-lead Leadless Array (LAP) and 8-lead SAP packages. In addition, the entire family is available in 2.7V (2.7V to 5.5V) versions.

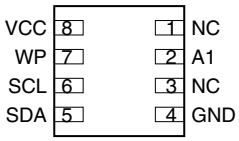
Table 1. Pin Configurations

Pin Name	Function
A1	Address Input
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
NC	No Connect

8-lead PDIP

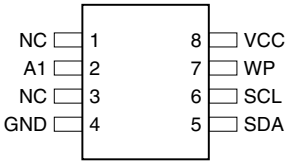


8-lead Leadless Array

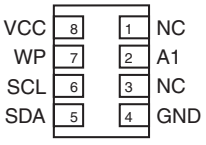


Bottom View

8-lead SOIC



8-lead SAP



Bottom View

Two-wire Serial EEPROM

1M (131,072 x 8)

AT24C1024(1)

Note: 1. Not recommended for new design; please refer to AT24C1024B datasheet.

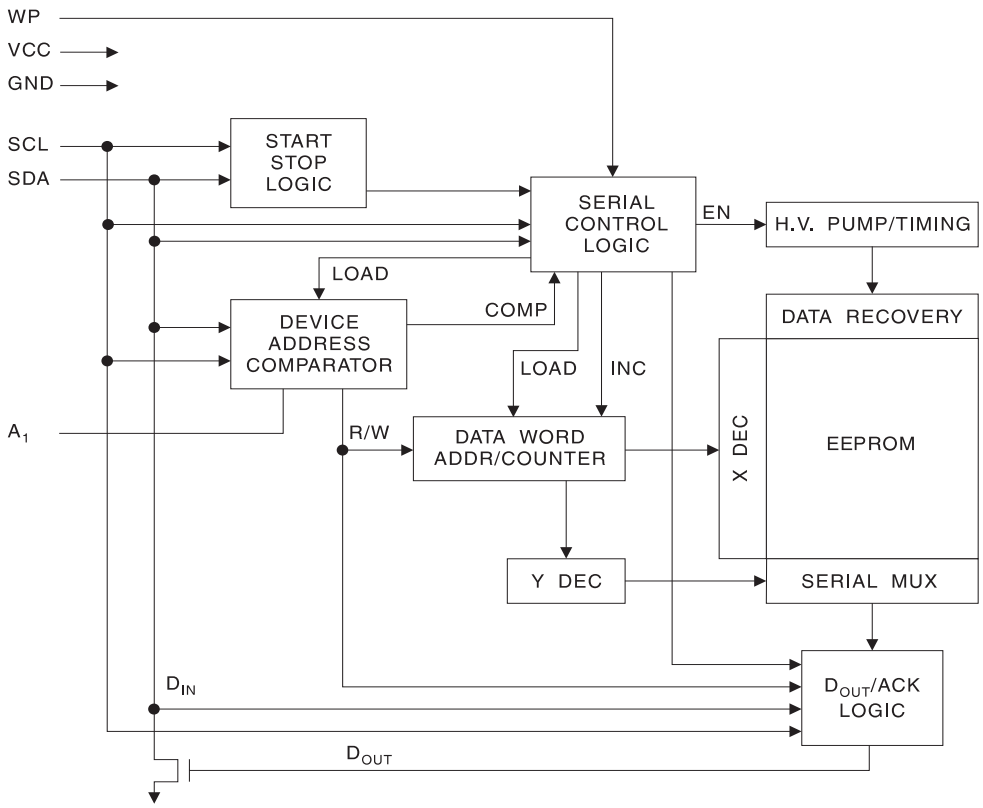
Rev. 1471O–SEEPR–3/07

Absolute Maximum Ratings*

Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Voltage on Any Pin with Respect to Ground	–1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 1. Block Diagram



Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bi-directional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open-collector devices.

DEVICE/ADDRESSES (A1): The A1 pin is a device address input that can be hardwired or left not connected for hardware compatibility with other AT24Cxx devices. When the A1 pin is hardwired, as many as two 1024K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section). If the A1 pin is left floating, the A1 pin will be internally pulled down to GND if the capacitive coupling to the circuit board V_{CC} plane is <3 pF. If coupling is >3 pF, Atmel recommends connecting the A1 pin to GND.

WRITE PROTECT (WP): The write protect input, when connected to GND, allows normal write operations. When WP is connected high to V_{CC}, all write operations to the memory are inhibited. If the pin is left floating, the WP pin will be internally pulled down to GND if the capacitive coupling to the circuit board V_{CC} plane is <3 pF. If coupling is >3 pF, Atmel recommends connecting the pin to GND. Switching WP to V_{CC} prior to a write operation creates a software write-protect function.

Memory Organization

AT24C1024, 1024K SERIAL EEPROM: The 1024K is internally organized as 512 pages of 256 bytes each. Random word addressing requires a 17-bit data word address.

Table 2. Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +2.7V

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (A_1, SCL)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

Table 3. DC Characteristics

Applicable over recommended operating range from: T_{AI} = –40°C to +85°C, V_{CC} = +2.7V to +5.5V, T_{AC} = 0°C to +70°C, V_{CC} = +2.7V to +5.5V (unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC}	Supply Voltage			2.7		5.5	V
I_{CC}	Supply Current	V_{CC} = 5.0V	READ at 400 kHz			2.0	mA
I_{CC}	Supply Current	V_{CC} = 5.0V	WRITE at 400 kHz			5.0	mA
I_{SB}	Standby Current	V_{CC} = 2.7V	V_{IN} = V_{CC} or V_{SS}			3.0	µA
		V_{CC} = 5.5V				6.0	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}			0.10	3.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}			0.05	3.0	µA
V_{IL}	Input Low Level[1]			–0.6		V_{CC} x 0.3	V
V_{IH}	Input High Level[1]			V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Level	V_{CC} = 3.0V	I_{OL} = 2.1 mA			0.4	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

Table 4. AC Characteristics[1]

Applicable over recommended operating range from T_A = –40°C to +85°C, V_{CC} = +2.7V to +5.5V, C_L = 100 pF (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Max	Units
f_{SCL}	Clock Frequency, SCL	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$		1000 400	kHz
t_{LOW}	Clock Pulse Width Low	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$	0.4 1.3		µs
t_{HIGH}	Clock Pulse Width High	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$	0.4 0.6		µs
t_{AA}	Clock Low to Data Out Valid	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$	0.05 0.05	0.55 0.9	µs
t_{BUF}	Time the bus must be free before a new transmission can start[2]	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$	0.5 1.3		µs
$t_{HD.STA}$	Start Hold Time	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$	0.25 0.6		µs
$t_{SU.STA}$	Start Setup Time	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$	0.25 0.6		µs
$t_{HD.DAT}$	Data In Hold Time		0		µs
$t_{SU.DAT}$	Data In Setup Time		100		ns
t_R	Inputs Rise Time[2]			0.3	µs
t_F	Inputs Fall Time[2]	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$		100 300	ns
$t_{SU.STO}$	Stop Setup Time	$4.5V \le V_{CC} \le 5.5V$ $2.7V \le V_{CC} \le 5.5V$	0.25 0.6		µs
t_{DH}	Data Out Hold Time		50		ns
t_{WR}	Write Cycle Time			10	ms
Endurance[2]	5.0V, 25°C, Page Mode		100K		Write Cycles

Notes: 1. AC measurement conditions:
R_L (connects to V_{CC}): 1.3 kΩ (2.7V, 5V)
Input pulse voltages: 0.3 V_{CC} to 0.7 V_{CC}
Input rise and fall times: ≤50 ns
Input and output timing reference voltages: 0.5 V_{CC}
2. This parameter is ensured by characterization only.

Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see Figure 4 on page 7). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see Figure 5 on page 8).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the Stop command will place the EEPROM in a standby power mode (see Figure 5 on page 8).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero during the ninth clock cycle to acknowledge that it has received each word.

STANDBY MODE: The AT24C1024 features a low-power standby mode which is enabled: a) upon power-up and b) after the receipt of the stop bit and the completion of any internal operations.

MEMORY RESET: After an interruption in protocol, power loss or system reset, any two-wire part can be reset by following these steps:

1. Clock up to 9 cycles.
2. Look for SDA high in each cycle while SCL is high.
3. Create a start condition.

Device Power Up And Power Down Recommendation

POWER UP: It is recommended to power up from 0V to full VCC in less than 1ms and then hold for at least 100µs at full VCC level before first operation.

POWER DOWN: It is recommended to power down from full VCC to 0V in less than 1ms and then hold at 0V for at least 0.5s before power up. It is not recommended to VCC power down to non-zero volt and then slowly go to zero volt.

Figure 2. Bus Timing (SCL: Serial Clock, SDA: Serial Data I/O®)

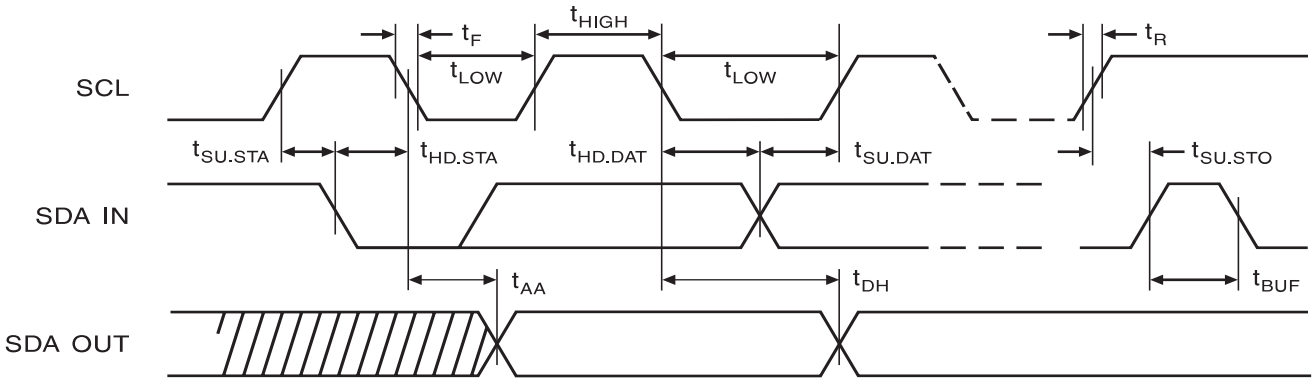
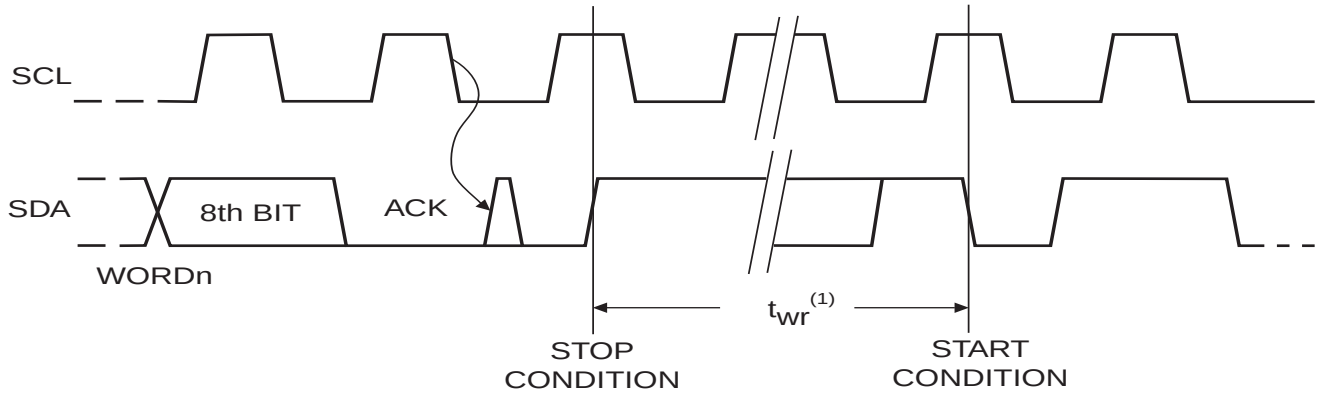


Figure 3. Write Cycle Timing (SCL: Serial Clock, SDA: Serial Data I/O)



Note: 1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

Figure 4. Data Validity

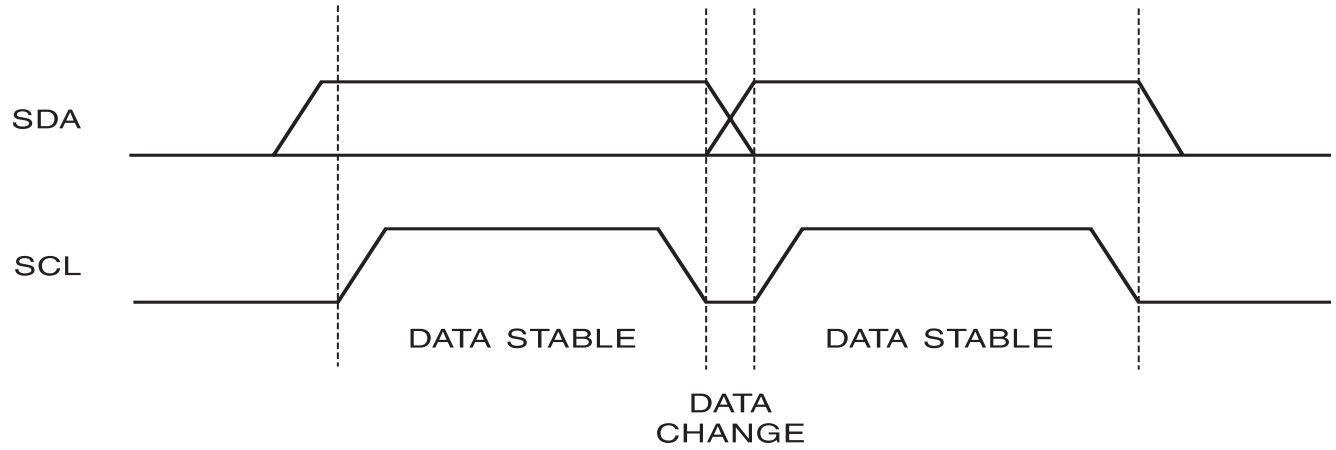


Figure 5. Start and Stop Definition

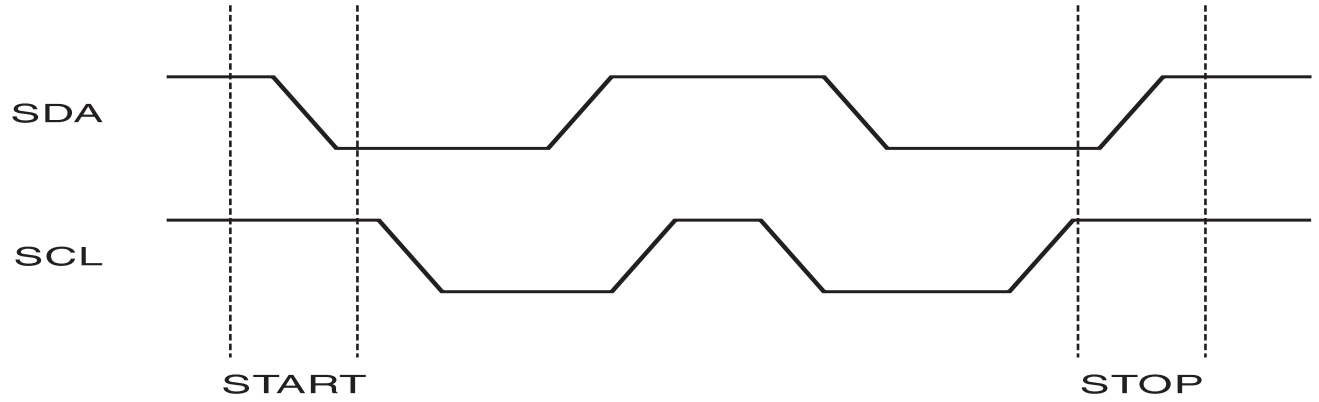
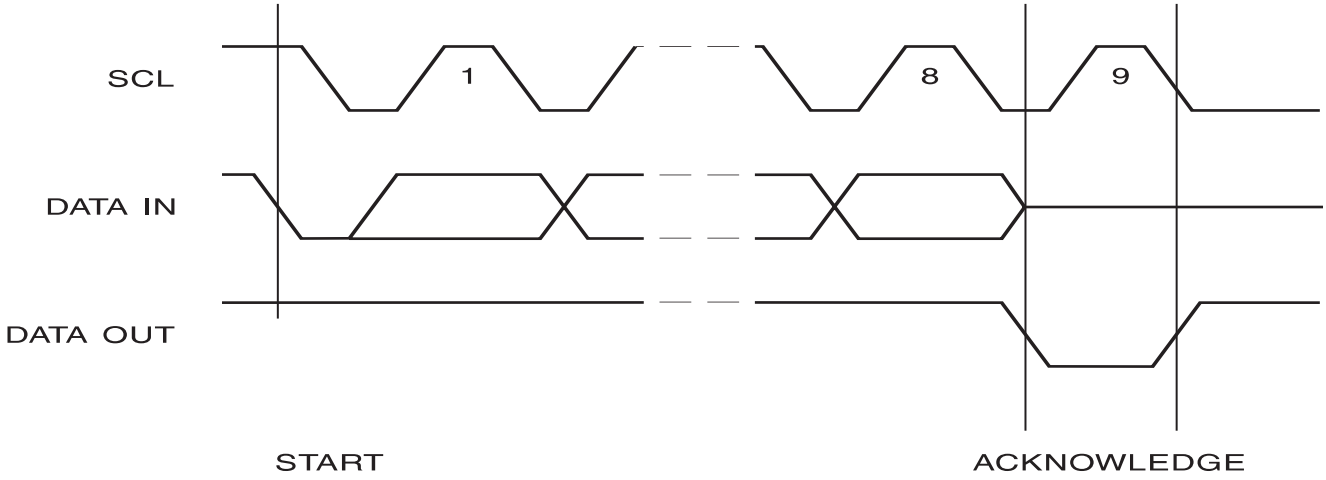


Figure 6. Output Acknowledge



Device Addressing

The 1024K EEPROM requires an 8-bit device address word following a start condition to enable the chip for a read or write operation (see Figure 7 on page 11). The device address word consists of a mandatory one, zero sequence for the first five most significant bits as shown. This is common to all two-wire EEPROM devices.

The 1024K uses the one device address bit, A1, to allow up to two devices on the same bus. The A1 bit must compare to the corresponding hardwired input pin. The A1 pin uses an internal proprietary circuit that biases it to a logic low condition if the pin is allowed to float.

The seventh bit (P_0) of the device address is a memory page address bit. This memory page address bit is the most significant bit of the data word address that follows. The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a zero. If a compare is not made, the device will return to a standby state.

DATA SECURITY: The AT24C1024 has a hardware data protection scheme that allows the user to write-protect the entire memory when the WP pin is at V_{CC}.

Write Operations

BYTE WRITE: To select a data word in the 1024K memory requires a 17-bit word address. The word address field consists of the P_0 bit of the device address, then the most significant word address followed by the least significant word address (see Figure 8 on page 11)

A write operation requires the P_0 bit and two 8-bit data word addresses following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero. The addressing device, such as a microcontroller, then must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle, T_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see Figure 8 on page 11).

PAGE WRITE: The 1024K EEPROM is capable of 256-byte page writes.

A page write is initiated the same way as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 255 more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (see Figure 9 on page 11).

The data word address lower 8 bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 256 data words are transmitted to the EEPROM, the data word address will “roll over” and previous data will be overwritten. The address “rollover” during write is from the last byte of the current page to the first byte of the same page.

ACKNOWLEDGE POLLING: Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero, allowing the read or write sequence to continue.

Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "rollover" during read is from the last byte of the last memory page, to the first byte of the first page.

Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following stop condition (see Figure 10 on page 11).

RANDOM READ: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition (see Figure 11 on page 12).

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a zero, but does generate a following stop condition (see Figure 12 on page 12).

Figure 7. Device Address

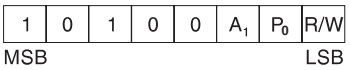


Figure 8. Byte Write

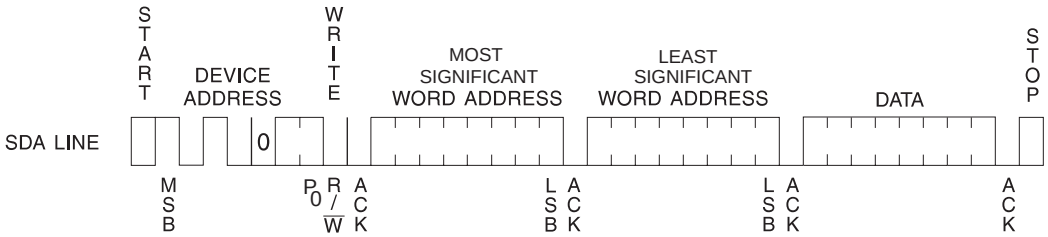


Figure 9. Page Write

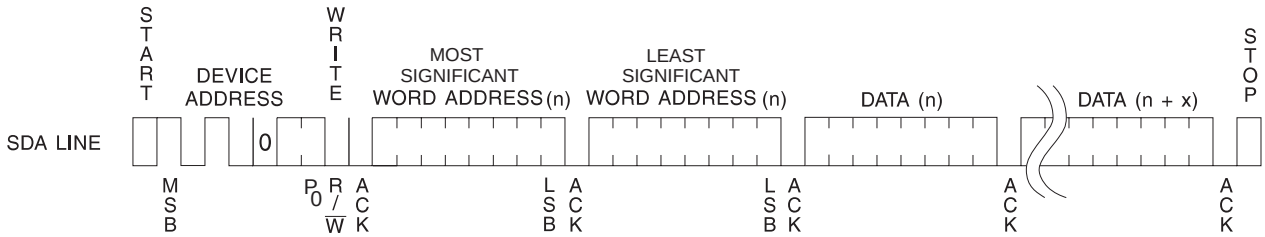


Figure 10. Current Address Read

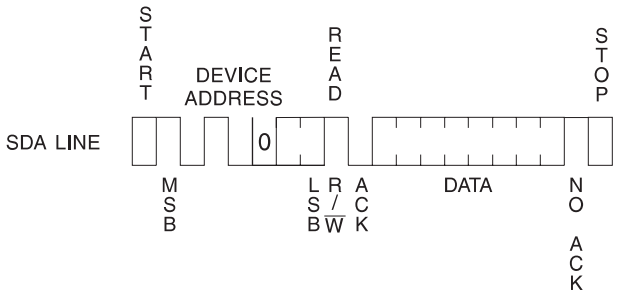


Figure 11. Random Read

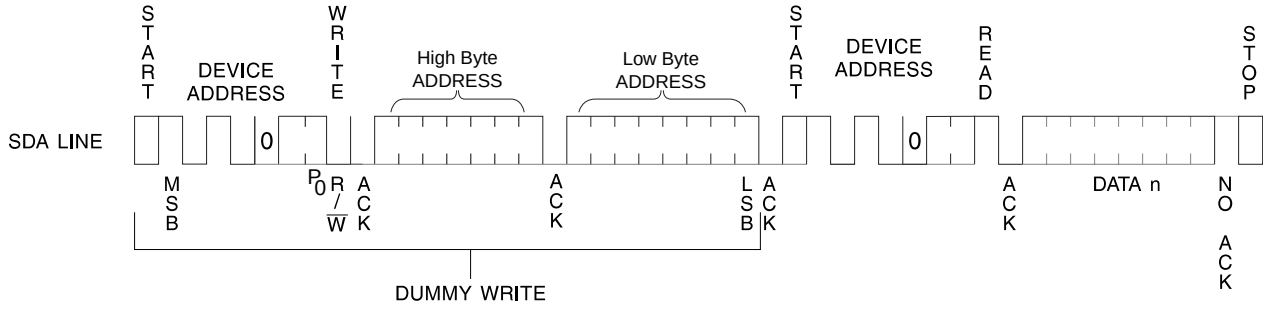
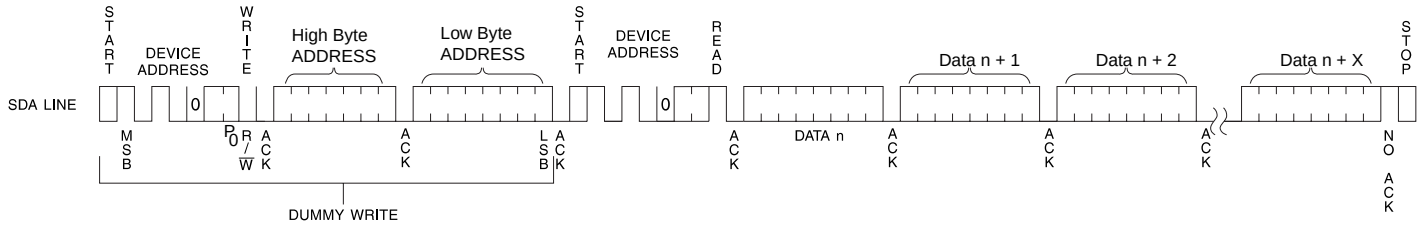


Figure 12. Sequential Read



Ordering Information[1]

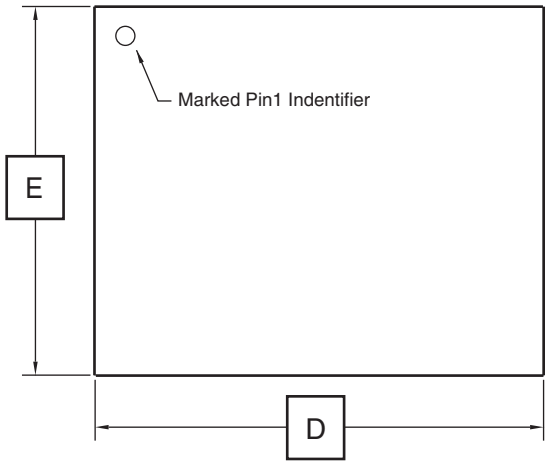
Ordering Code	Package	Operation Range
AT24C1024C1-10CU-2.7[2]	8CN1	Lead-free/Halogen-free/ Industrial Temperature (–40°C to 85°C)
AT24C1024-10PU-2.7[2]	8P3	
AT24C1024W-10SU-2.7[2]	8S2	
AT24C1024Y4-10YU-2.7[2]	8Y4	
AT24C1024-W2.7-11[3]	Die Sale	Industrial Temperature (–40°C to 85°C)

Notes:
1. This device is not recommended for new design. Please refer to AT24C1024B datasheet. For 2.7V devices used in the 4.5V to 5.5V range, please refer to performance values in the AC and DC Characteristics tables.
2. "U" designates Green Package & RoHS compliant.
3. Available in waffle pack and wafer form; order as SL788 for wafer form. Bumped die available upon request. Please contact Serial EEPROM Marketing.

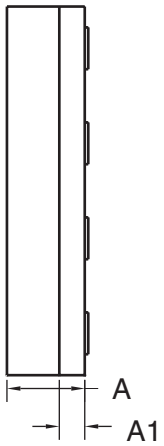
Package Type	
8CN1	8-lead, 0.300" Wide, Leadless Array Package (LAP)
8P3	8-lead, 0.300" Wide, Plastic Dual In-line Package (PDIP)
8S2	8-lead, 0.200" Wide, Plastic Gull Wing Small Outline Package (EIAJ SOIC)
8Y4	8-lead, (6.00 x 4.90 mm Body) SOIC Array Package (SAP)
Options	
–2.7	Low Voltage (2.7V to 5.5V)

Packaging Information

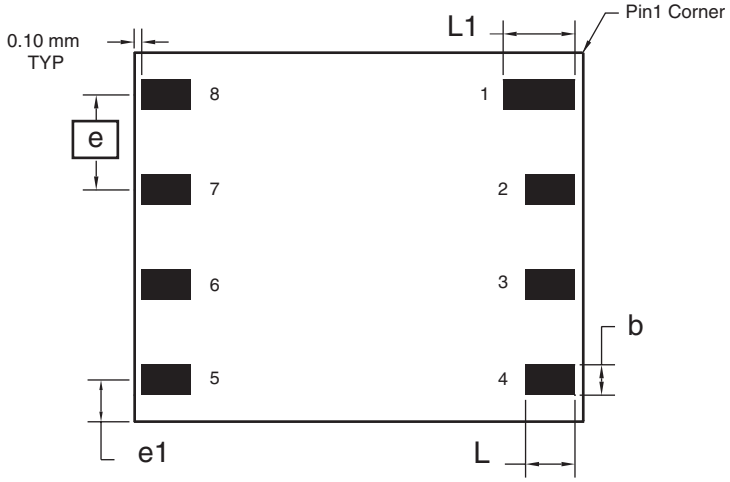
8CN1 – LAP



Top View



Side View



Bottom View

COMMON DIMENSIONS
(Unit of Measure = mm)

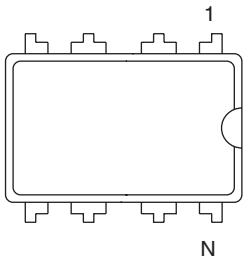
SYMBOL	MIN	NOM	MAX	NOTE
A	0.94	1.04	1.14	
A1	0.30	0.34	0.38	
b	0.36	0.41	0.46	1
D	7.90	8.00	8.10	
E	4.90	5.00	5.10	
e	1.27 BSC			
e1	0.60 REF			
L	0.62	.0.67	0.72	1
L1	0.92	0.97	1.02	1

Note: 1. Metal Pad Dimensions.

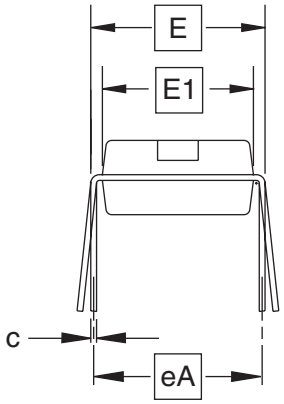
11/13/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**8CN1**, 8-lead (8 x 5 x 1.04 mm Body), Lead Pitch 1.27 mm, Leadless Array Package (LAP)	8CN1	A

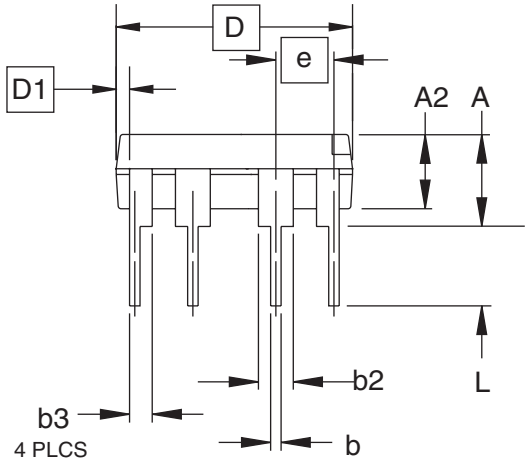
8P3 – PDIP



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = inches)

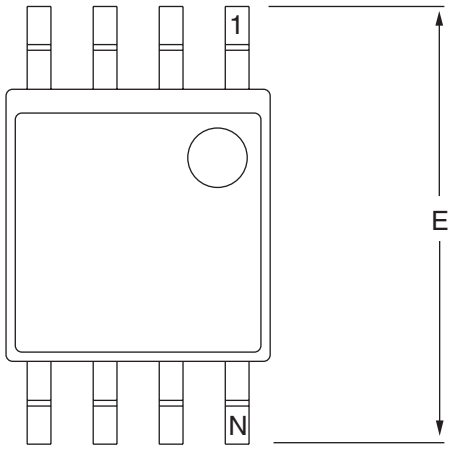
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	0.210	2
A2	0.115	0.130	0.195	
b	0.014	0.018	0.022	5
b2	0.045	0.060	0.070	6
b3	0.030	0.039	0.045	6
c	0.008	0.010	0.014	
D	0.355	0.365	0.400	3
D1	0.005	–	–	3
E	0.300	0.310	0.325	4
E1	0.240	0.250	0.280	3
e	0.100 BSC			
eA	0.300 BSC			4
L	0.115	0.130	0.150	2

Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-001, Variation BA, for additional information.
2. Dimensions A and L are measured with the package seated in JEDEC seating plane Gauge GS-3.
3. D, D1 and E1 dimensions do not include mold Flash or protrusions. Mold Flash or protrusions shall not exceed 0.010 inch.
4. E and eA measured with the leads constrained to be perpendicular to datum.
5. Pointed or rounded lead tips are preferred to ease insertion.
6. b2 and b3 maximum dimensions do not include Dambar protrusions. Dambar protrusions shall not exceed 0.010 (0.25 mm).

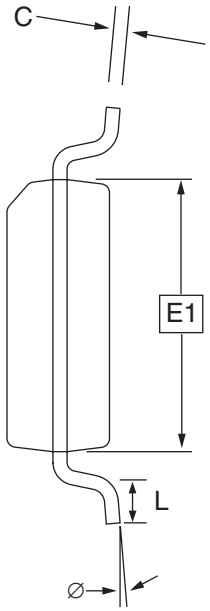
01/09/02

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**8P3**, 8-lead, 0.300" Wide Body, Plastic Dual In-line Package (PDIP)	8P3	B

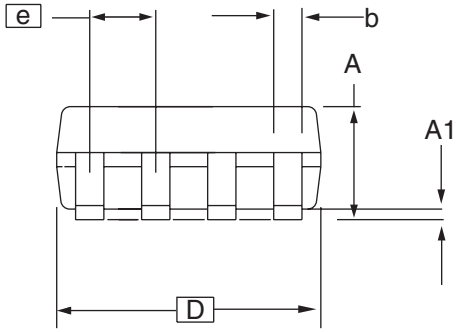
8S2 – EIAJ SOIC



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

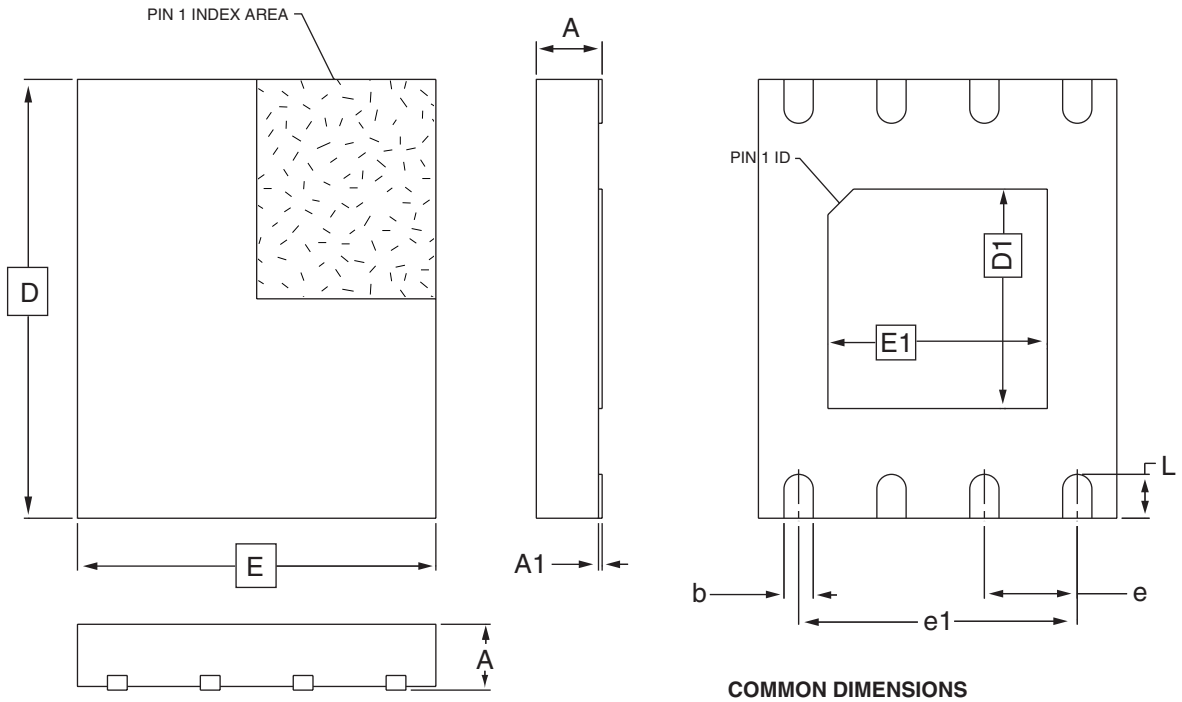
SYMBOL	MIN	NOM	MAX	NOTE
A	1.70		2.16	
A1	0.05		0.25	
b	0.35		0.48	5
C	0.15		0.35	5
D	5.13		5.35	
E1	5.18		5.40	2, 3
E	7.70		8.26	
L	0.51		0.85	
∅	0°		8°	
e	1.27 BSC			4

Notes: 1. This drawing is for general information only; refer to EIAJ Drawing EDR-7320 for additional information.
2. Mismatch of the upper and lower dies and resin burrs are not included.
3. It is recommended that upper and lower cavities be equal. If they are different, the larger dimension shall be regarded.
4. Determines the true geometric position.
5. Values b and C apply to pb/Sn solder plated terminal. The standard thickness of the solder layer shall be 0.010 +0.010/–0.005 mm.

10/7/03

2325 Orchard Parkway San Jose, CA 95131	**TITLE** **8S2**, 8-lead, 0.209" Body, Plastic Small Outline Package (EIAJ)	**DRAWING NO.** 8S2	**REV.** C

8Y4 – SAP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	0.90	
A1	0.00	–	0.05	
D	5.80	6.00	6.20	
E	4.70	4.90	5.10	
D1	2.85	3.00	3.15	
E1	2.85	3.00	3.15	
b	0.35	0.40	0.45	
e		1.27 TYP		
e1		3.81 REF		
L	0.50	0.60	0.70	

5/24/04

1150 E. Cheyenne Mtn. Blvd. Colorado Springs, CO 80906	**TITLE** **8Y4**, 8-lead (6.00 x 4.90 mm Body) SOIC Array Package (SAP) Y4	**DRAWING NO.** 8Y4	**REV.** A

Revision History

Doc. Rev.	Date	Comments
1471O	3/2007	Implemented revision history. Added ‘Not recommended for new design; please refer to AT24C1024B datasheet’ note to page 1 and page 13.

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